From: Carl Bruggeman (bruggema@cs.indiana.edu) Search Result 3
Subject: Question about **processor cache**-line spares
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Date: 1994-08-30 17:16:45 PST Original Format

I posted this message to comp.arch about a week ago and I got only two replies (thanks David and John!), so I am trying again in the hope that this news group might be more appropriate...

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I have a few question about **cache** design for on-chip **processor** caches. I vaguely recall hearing that on-chip caches can be designed with extra **cache**-lines that can replace defective **cache** lines (during testing, I believe) in order to increase **processor** yields.

1. Are spare **cache** lines that can be spliced in to replace defective lines ever/sometimes/always used in todays processors (especially designs with large caches like the Alpha and Power-PC)?

2. Since first level **cache** access times are usually one of the most important factors limiting **processor** cycle time, does sparing have any impact on **cache** cycle time? Only when a spare is actually spliced in? Even when a spare isn't spliced in?

3. I know that defects rates are closely guarded secrets, but is there anything in the literature about the effectiveness of **cache** line spares?

On the related subject of defects and yields...

If I remember correctly from my graduate-level VLSI course where we used a simple 2 metal process (my only source of VLSI knowledge), vias, especially vias to the second-level metal, were supposed to contribute a fair amount to the likely-hood of defects and lower yields. Assuming this has any basis in reality, it seems to me that the 3-level and 4-levels of metal used in todays high-end **processor** would also have a substantial negative impact on yields. Is this the case?

Thanks in advance for any information, insights, or references!

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| 7 | 0 | voltage near4 indicat$6 with supply and g06f$.ipc. | IBM_TDB | 2003/10/08 10:37 |
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